WHAT IS CLAIMED IS:

1. An oversampling clock recovery method comprising the steps of:

generating non-uniform multi-phase clock signals having a non-uniform interval, said non-uniform multi-phase clock signals comprising three or more phase clock signals for one bit of an input data;

controlling a phase of said non-uniform multi-phase clock signals so that a phase of one of two edges in two-phase clock signals having a relative narrower interval among said non-uniform multi-phase clock signals is locked with a phase of a transition point of said input data;

digitally controlling, by using selection circuits and delay locked loops each comprising a plurality of delay buffers, phases of two or more sets of uniform multi-phase clock signals having a uniform interval at a resolution less than a propagation delay of a delay buffer in said delay locked loops;

keeping, by said digital control, a phase difference between a set of uniform multi-phase clock signals and another set of uniform multi-phase clock signals to a phase difference shorter than said propagation delay; and

using a combination of said two or more sets of uniform multi-phase clock signals as said non-uniform multi-phase clock signals.

2. An oversampling clock recovery method as claimed in claim 1, wherein said non-uniform multi-phase clock signals comprises three-phase clock signals for one bit of said input data.

3. An oversampling clock recovery method as claimed in claim 1, wherein said step of controlling the phase of said non-uniform multi-phase clock signals is carried out by using a digital phase control method which comprises the steps of:

preparing first multi-phase clock signals having a fixed phase and having a first uniform phase interval;

preparing second multi-phase clock signals having a second uniform phase interval different from said first uniform phase interval;

phase locking a specific clock signal in said first multi-phase clock signals and a particular clock signal in said second multi-phase clock signals; and

changing a combination of the specific and the particular clock signals to be phase-locked to shift a phase of second multi-phase clock signals.

4. An oversampling clock recovery method as claimed in claim 1, wherein said step of controlling the phase of said non-uniform multi-phase clock signals is carried out by a digital phase control method which comprises the steps of:

preparing first multi-phase clock signals having a fixed phase and having a first uniform phase interval;

preparing second multi-phase clock signals having a second uniform phase interval different from said first uniform phase interval;

preparing third multi-phase clock signals having the second uniform phase interval;

phase locking a specific clock signal in said first multi-phase clock signals and a first particular clock signal in said second multi-phase clock signals;

phase locking a specific clock signal in said first multi-phase clock signals and a second particular clock signal in said third multi-phase clock signals; and

changing a combination of the specific clock signal and the first particular clock signal to be phase-locked and a combination of the specific clock signal and the second particular clock signal to be phase-

locked, thereby controlling phases of said second and said third multi-phase clock signals for use in sampling said input data with a phase difference between said second multi-phase clock signals and said third multi-phase clock signals kept.

5. An oversampling clock recovery method as claimed in claim 4, wherein the resolution for controlling the phases of said second and said third multi-phase clock signals is equal to the phase difference between said second multi-phase clock signals and said third multi-phase clock signals.

6. An oversampling clock recovery method comprising the steps of:

generating compression multi-phase clock signals having condensation and rarefaction in arrangement, said compression multi-phase clock signals comprising three or more phase clock signals for one bit of an input data, said compression multi-phase clock signals having a compression period equal to a length of one bit in said input data;

controlling a phase of said compression multi-phase clock signals so that a phase of one of clock edges in two clock signals having a condensation portion among said compression multi-phase clock signals is phase locked with a phase of a transition point of said input data;

digitally controlling, by using selection circuits and delay locked loops each comprising a plurality of delay buffers, phases of two or more sets of uniform multi-phase clock signals having uniform interval at a resolution shorter than a propagation delay of a delay buffer in said delay locked loops;

keeping, by said digital control, a phase difference between a set of uniform multi-phase clock signals and another set of uniform

multi-phase clock signals to a phase difference shorter than said propagation delay; and

using a combination of said two or more sets of uniform multi-phase clock signals as said compression multi-phase clock signals.

7. An oversampling clock recovery method as claimed in claim 6, wherein said compression multi-phase clock signals comprises three-phase clock signals for one bit for said input data.

8. An oversampling clock recovery method as claimed in claim 6, wherein said step of controlling the phase of said compression multi-phase clock signals is carried out by using a digital phase control method which comprises the steps of:

preparing first multi-phase clock signals having a fixed phase and having a first uniform phase interval;

preparing second multi-phase clock signals having a second uniform phase interval different from said first uniform phase interval;

phase locking a specific clock signal in said first multi-phase clock signals and a particular clock signal in said second multi-phase clock signals; and

changing a combination of the specific and the particular clock signals to be phase-locked to shift a phase of second multi-phase clock signals.

9. An oversampling clock recovery method as claimed in claim 6, wherein said step of controlling the phase of said compression multi-phase clock signals is carried out by a digital phase control method which comprises the steps of:

preparing first multi-phase clock signals having a fixed phase and having a first uniform phase interval;

preparing second multi-phase clock signals having a second uniform phase interval different from said first uniform phase interval;

preparing third multi-phase clock signals having the second uniform phase interval;

phase locking a specific clock signal in said first multi-phase clock signals and a first particular clock signal in said second multi-phase clock signals;

phase locking a specific clock signal in said first multi-phase clock signals and a second particular clock signal in said third multi-phase clock signals; and

changing a combination of the specific clock signal and the first particular clock signal to be phase-locked and a combination of the specific clock signal and the second particular clock signal to be phase-locked, thereby controlling phases of said second and said third multi-phase clock signals for use in sampling said input data with a phase difference between said second multi-phase clock signals and said third multi-phase clock signals kept.

10. An oversampling clock recovery method as claimed in claim 9, wherein the resolution for controlling the phases of said second and said third multi-phase clock signals is equal to the phase difference between said second multi-phase clock signals and said third multi-phase clock signals.

11. An oversampling clock recovery method comprising the steps of:

generating non-uniform multi-phase clock signals having a non-uniform interval, said non-uniform multi-phase clock signals comprising four or more phase clock signals for one bit of an input data;

controlling a phase of said non-uniform multi-phase clock signals so that a phase of one of two clock edges in a first set of clock signals having a relative narrower interval among said non-uniform multi-phase clock signals is phase locked with a phase of a transition

point of said input data; and

controlling a phase of said non-uniform multi-phase clock signals so as to avoid making a phase of one of two clock edges in a second set of clock signals having a relative narrower interval among said non-uniform multi-phase clock signals phase lock with the phase of the transition point of said input data, said second set of clock signals being apart from said first set of clock signals through a relatively wider phase interval by about a length of half bit of said input data.

12. An oversampling clock recovery method as claimed in claim 11, wherein said non-uniform multi-phase clock signals comprises four-phase clock signals for one bit for said input data.

13. An oversampling clock recovery method as claimed in claim 11, wherein further comprises the steps of:

digitally controlling, by using selection circuits and delay locked loops each comprising a plurality of delay buffers, phases of two or more sets of uniform multi-phase clock signals having uniform interval at a resolution shorter than a propagation delay of a delay buffer in said delay locked loops;

keeping, by said digital control, a phase difference between a set of uniform multi-phase clock signals and another set of uniform multi-phase clock signals to a phase difference shorter than said propagation delay; and

using a combination of said two or more sets of uniform multi-phase clock signals as said non-uniform multi-phase clock signals.

14. An oversampling clock recovery method as claimed in claim 11, wherein said step of controlling the phase of said non-uniform multi-phase clock signals is carried out by using a digital phase control method which comprises the steps of:

preparing first multi-phase clock signals having a fixed phase

and having a first uniform phase interval;

preparing second multi-phase clock signals having a second uniform phase interval different from said first uniform phase interval;

phase locking a specific clock signal in said first multi-phase clock signals and a particular clock signal in said second multi-phase clock signals; and

changing a combination of the specific and the particular clock signals to be phase-locked to shift a phase of second multi-phase clock signals.

15. An oversampling clock recovery method as claimed in claim 11, wherein said step of controlling the phase of said non-uniform multi-phase clock signals is carried out by a digital phase control method which comprises the steps of:

preparing first multi-phase clock signals having a fixed phase and having a first uniform phase interval;

preparing second multi-phase clock signals having a second uniform phase interval different from said first uniform phase interval;

preparing third multi-phase clock signals having the second uniform phase interval;

phase locking a specific clock signal in said first multi-phase clock signals and a first particular clock signal in said second multi-phase clock signals;

phase locking a specific clock signal in said first multi-phase clock signals and a second particular clock signal in said third multi-phase clock signals; and

changing a combination of the specific clock signal and the first particular clock signal to be phase-locked and a combination of the specific clock signal and the second particular clock signal to be phase-locked, thereby controlling phases of said second and said third multi-

phase clock signals for use in sampling said input data with a phase difference between said second multi-phase clock signals and said third multi-phase clock signals kept.

16. An oversampling clock recovery method as claimed in claim 15, wherein the resolution for controlling the phases of said second and said third multi-phase clock signals is equal to the phase difference between said second multi-phase clock signals and said third multi-phase clock signals.

17. An oversampling clock recovery method comprising the steps of:

generating compression multi-phase clock signals having condensation and rarefaction in arrangement, said compression multi-phase clock signals comprising four or more phase clock signals for one bit of an input data, said compression multi-phase clock signals having a compression period equal to one-second of a length of one bit in said input data;

controlling a phase of said compression multi-phase clock signals so that a phase of one of two clock edges in a first set of clock signals having a condensation portion among said compression multi-phase clock signals is phase locked with a phase of a transition point of said input data; and

controlling a phase of said non-uniform multi-phase clock signals so as to avoid making a phase of one of two clock edges in a second set of clock signals having a condensation portion among said non-uniform multi-phase clock signals phase lock with the phase of the transition point of said input data, said second set of clock signals being adjacent to said first set of clock signals through a rarefaction portion.

18. An oversampling clock recovery method as claimed in claim 17, wherein said compression multi-phase clock signals comprises

four-phase clock signals for one bit for said input data.

19. An oversampling clock recovery method as claimed in claim 17, wherein further comprises the steps of:

digitally controlling, by using selection circuits and delay locked loops each comprising a plurality of delay buffers, phases of two or more sets of uniform multi-phase clock signals having uniform interval at a resolution shorter than a propagation delay of a delay buffer in said delay locked loops;

keeping, by said digital control, a phase difference between a set of uniform multi-phase clock signals and another set of uniform multi-phase clock signals to a phase difference shorter than said propagation delay; and

using a combination of said two or more sets of uniform multi-phase clock signals as said compression multi-phase clock signals.

20. An oversampling clock recovery method as claimed in claim 17, wherein said step of controlling the phase of said compression multi-phase clock signals is carried out by using a digital phase control method which comprises the steps of:

preparing first multi-phase clock signals having a fixed phase and having a first uniform phase interval;

preparing second multi-phase clock signals having a second uniform phase interval different from said first uniform phase interval;

phase locking a specific clock signal in said first multi-phase clock signals and a particular clock signal in said second multi-phase clock signals; and

changing a combination of the specific and the particular clock signals to be phase-locked to shift a phase of second multi-phase clock signals.

21. An oversampling clock recovery method as claimed in

claim 17, wherein said step of controlling the phase of said compression multi-phase clock signals is carried out by a digital phase control method which comprises the steps of:

preparing first multi-phase clock signals having a fixed phase and having a first uniform phase interval;

preparing second multi-phase clock signals having a second uniform phase interval different from said first uniform phase interval;

preparing third multi-phase clock signals having the second uniform phase interval;

phase locking a specific clock signal in said first multi-phase clock signals and a first particular clock signal in said second multi-phase clock signals;

phase locking a specific clock signal in said first multi-phase clock signals and a second particular clock signal in said third multi-phase clock signals; and

changing a combination of the specific clock signal and the first particular clock signal to be phase-locked and a combination of the specific clock signal and the second particular clock signal to be phase-locked, thereby controlling phases of said second and said third multi-phase clock signals for use in sampling said input data with a phase difference between said second multi-phase clock signals and said third multi-phase clock signals kept.

22. An oversampling clock recovery method as claimed in claim 21, wherein the resolution for controlling the phases of said second and said third multi-phase clock signals is equal to the phase difference between said second multi-phase clock signals and said third multi-phase clock signals.

23. An oversampling clock recovery circuit comprising:

a first delay locked loop comprising m-stage delay buffers

where m represents a first positive integer which is not less than two;

a first selection circuit for selecting, as a first selected delay buffer, a first one of said m-stage delay buffers in said first delay locked loop to pick up a first selected clock signal from said first selected delay buffer;

a second selection circuit for selecting, as a second selected delay buffer, a second one of said m-stage delay buffers in said first delay locked loop to pick up a second selected clock signal from said second selected delay buffer;

a second delay locked loop comprising n-stage delay buffers where n represents a second positive integer which is different from the first positive integer and which is not less than two;

a third selection circuit for selecting, as a third selected delay buffer, one of said n-stage delay buffers in said second delay locked loop to supply said third selected delay buffer with said first selected clock signal;

a third delay locked loop comprising n-stage delay buffers

a fourth selection circuit for selecting, as a fourth selected delay buffer, one of said n-stage delay buffers in said third delay locked loop to supply said fourth selected delay buffer with said second selected clock signal;

a phase comparison portion for sampling an input data using both clock signals produced by said second delay locked loop and clock signals produced by said third delay locked loop to detect lag/lead of said clock signals in reference with said input data, said phase comparison portion producing a comparison result indicative of the lag/lead of said clock signals; and

a control circuit for controlling said first through said fourth selection circuits on the basis of said comparison result.

24. An oversampling clock recovery circuit as claimed in claim 23, wherein resolution of a phase control is set so as to be smaller than a propagation delay in said delay buffers, said control circuit carrying out the phase control so as to differ by one resolution between said first and said third selection circuits and said second and said fourth selection circuits.

25. An oversampling clock recovery circuit as claimed in claim 23, wherein each of said second and said third delay locked loops comprises the n-stage delay buffers which are chained with each other in a ring-shaped fashion, said second delay locked loop compares phases of input and output signals in a first delay line having said third selected delay buffer as a first stage thereof, and said third delay locked loop compares phases of input and output signals in a second delay line having said fourth selected delay buffer as a first stage thereof.